THE SPGS-MODULE

Thermal measurements and simulations with a

Silicon Detector - **P**yrolytic **G**raphite **S**andwich *

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Abstract

We have conducted thermal measurements on a thermal prototype of a novel concept to construct silicon modules, using thermally conductive Pyrolytic Graphite as a heat spreader sandwiched between two single-sided silicon detectors. We have measured the temperature profile as a function of heating power at a coolant temperature of -10^{o}C and ambient temperatures of 0, -5, -10^{o}C and found that the temperature increase of the silicon detectors is below 3^{o}C for realistic power levels.

I. MOTIVATION

In future applications of silicon strip detectors at high luminosity colliders, thermal waste management will be of outmost importance. Due to comparable feature sizes, "modules" can be constructed consisting of silicon strip detectors with on-board front-end electronics (FEE) in the form of VLSI chips. For example in the silicon tracker for ATLAS, one of the experiments for the large hadron collider LHC, the modules contain two pairs of 6cmx6cm silicon detectors mounted back-to-back, with the VLSI chips mounted on hybrids, which straddle the detectors. In this way, the thermal waste management of detector and electronics becomes intimately connected. The maximum thermal power dissipation of an ATLAS module adds up to 3W with the FEE contributing 2mW/channel, for the FEE and 1W, i.e. $2.3*10^{-4}$ W/mm^3 due to self heating of the detectors after radiation damage. One aspect of the detector design lies in how to extract the heat with minimum thermal strains. These strains produce undesirable distortions in the very thin 300mm wafers, with an unpredictable impact on the detector resolution. The LHC silicon module concepts are composed of materials of very different coefficient of expansion (CTE) which exacerbates the thermal distortion problem. We propose a module design using highly thermally conductive materials arranged symmetrically, which minimizes thermal strains and avoids the thermal run-away problem.

Radiation damage in silicon detectors can produce significant increases in leakage current, with exponential temperature dependence [1]. A critical heating value is reached where the I$*$V power can no longer be conducted to the cooled region of the detector (“thermal run-away”) [2]. In single silicon detectors, this happens at a heat input of about $6.7*10^{-4}$W/cm^3 (see Fig. 1), only a safety factor of 2.9 over present predictions of the condition in ATLAS [3].

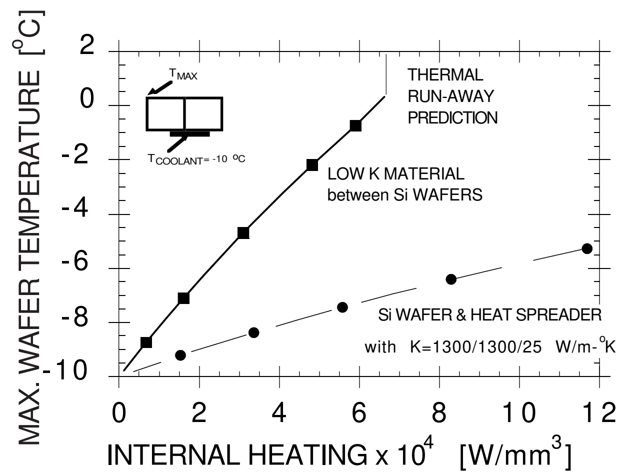

Fig. 1 Simulation of thermal run-away with and without heat spreader: maximum silicon temperature vs internal heating power of a single wafer.

We propose to avoid this problem by inserting a pyrolytic graphite (PG) heat spreader between the two single-sided silicon strip detectors, making a Silicon-PG Sandwich (SPGS) module. The PG we are using has a thermal conductivity of K = 1300w/m-^{o}K, about 10x that of silicon and approaching that of CVD diamond. The detector is cooled to -10^{o}C during operation, largely to avoid additional consequences of radiation damage (increase of depletion voltage). Besides preventing thermal run-away for all practical puposes, the PG material assures a highly uniform detector temperature, enhancing thermal stability, with a thermal gradient of less than 2^{o}C.

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II. CONSTRUCTION OF THE SPGS-MODULE PROTOTYPE

The principle of the SPGS-module is shown diagramatically in Fig.2: two single-sided silicon detectors of 300 µm thickness sandwich a so-called "heat spreader" of high thermal conductivity which conducts the heat generated both by the front-end electronics and by self-heating of the radiation damaged silicon detectors to the side, where the "EAR" connects to the cooling channel. In this series of measurements, we added a copper cooling block on top of the EAR and ran the liquid coolant through it. As we will see below, this allowed a reasonable constant temperature of the cooling block throughout the experiment, almost independent of the heating power.

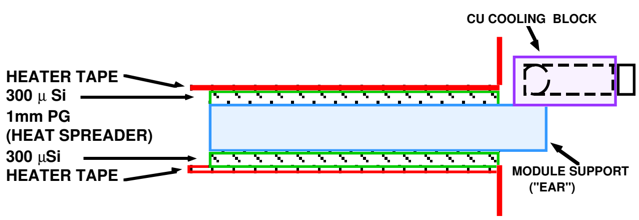

Fig. 2 Schematic of the SPGS-module

The heat spreader is a 1mm thick piece of Pyrolytic Graphite made by B.F. Goodrich, which has a thermal conductivity of 1300 W/m-^{o}K, and radiation length of 19cm. In order to minimize it's contribution to the material budget, we reduced the effective thickness with cut-outs as shown in Fig. 3: averaged over the 12cmx6cm active area, and including the EAR, this amounts to 720µm, about 0.37% of a radiation length, comparable to the contribution of one silicon detector of 300µm thickness. The asymmetric shape is chosen to have maximum heat conduction underneath the front-end electronics chips, which will be located to the right of the broken line in Fig. 3.

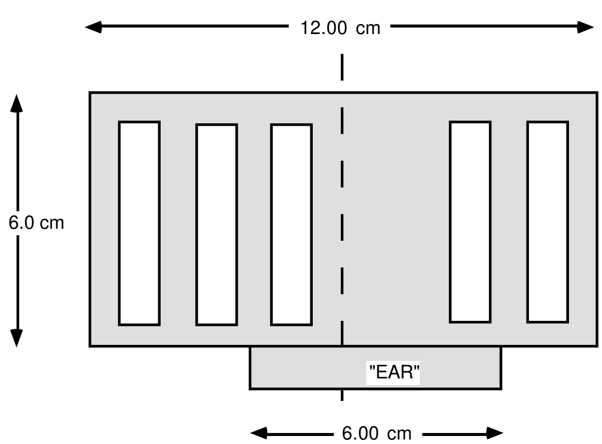

Fig. 3 Heat spreader made of pyrolytic graphite (PG). The cut-outs reduce the mass by 28%

Fig. 4 shows the thermal prototype including the location of the resistor temperature devices (RTD) used to measure the temperature profile. The front-end electronics contributes a predictable amount of heat of up to 3W to the module and is simulated by a Kapton based heater tape located across the module like in the widely tested r-ϕ modules [4,5]. The solid part of the PG heat spreader matches its location (Fig.3). All glue joints were made with 5min Epoxy. In order to prevent the air from being trapped in the cut-outs, we notched the PG pieces to allow the pressure to equalize with the environment.

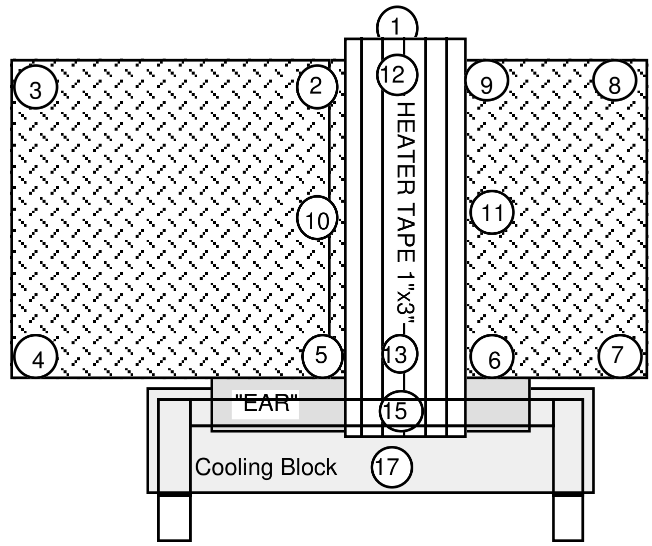

Fig. 4 Lay-out of the thermal prototype of the SPGS-module. The circled numbers indicate the location of RTD's to determine the temperature profile.

III.MEASUREMENTS

We used a total of 20 RTD's distributed over both surfaces of the module to map out the temperature profile. Fig. 4 shows the location of the RTD's glued to the top side. In addition, one RTD measured the ambient temperature. We had tested the RTD's before installation between -20 and +50^{o}C, and found them uniform to 0.1 Ω. In order to get immediate feed-back during the measurements, we used a computer controlled scanner (Keithley Model 706) and read the resistances from an electrometer (Keithley 617) directly into the computer with a LABVIEW program. We found out that we needed a settling time of about 10sec for the resistance readings to stabilize.

The measurements were performed in the cold box of the LBNL ATLAS Pixel group. The temperature of both the coolant (water-alcohol) and the ambient gas (LN_2 boil-off) were controlled independently. Since the leads of all RTD's were of the same length and the internal resistance of the scanner was finite but uniform, we expect all temperature sensors to behave uniformly. We performed a reading at room temperature and found the scatter of resistance values of the order 0.1^{o}C. The measurements of the temperature profile were performed at a coolant temperature of -10^{o}C, and ambient gas temperatures of -10, -5, and 0^{o}C, respectively.

A. Efficiency of Cooling

Fig 5 shows the temperature on the EAR (RTD#15) and the cooling block (RTD#17) as a function of the heater tape power for the three different ambient temperatures. Although the coolant was kept at a constant temperature, we observed a slight rise in cooling block temperature, which we will correct for below. Assuming that the convective heat input from ambient is proportional to the temperature difference between ambient and the silicon, we can determine the thermal resistance R between the EAR and the cooling block and the effective convection coefficient h_{conv} at the silicon surface. In Fig. 6, we show the temperature difference between the EAR and the cooling block, for ambient temperatures of T_{amb} = -10, -5 and 0^oC and coolant temperature of -10^oC. It can be expressed as a function of the heat input Q:

$$T_{EAR} - T_{Block} = Q*R + R*h_{conv}*A*\delta T, \qquad (1)$$

with $\delta T=T_{amb}-T_{EAR}-\Delta T$ the average temperature difference between the ambient gas and the silicon, ΔT being the temperature difference between the EAR and the silicon measured at every power setting and $\leq 3^oC$ based on the data shown below and A the total surface area. It should be noted, that during the first two low power settings at -10^oC, the ambient was close to -8^oC, thus convectively heating the module and causing the lower curve in Fig. 6 to deviate from a straight line through zero.

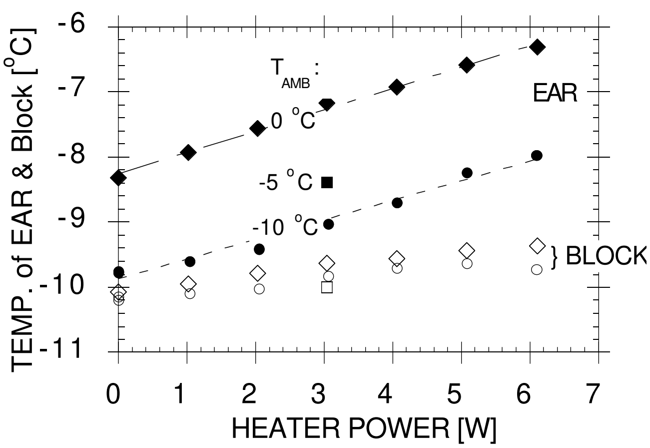

Fig. 5 Temperature of EAR and cooling block as a function of the heater tape power, at the three temperatures of the ambient gas, -10, -5 and 0^oC, and coolant at -10^oC.

Fitting the data in Fig. 6 with Eq. (1) yields the thermal resistance of the EAR relative to the block to R= 0.42 $^oK/W$, and the effective convection coefficient of the silicon h_{conv} = 30 $W/m^2/^oK$, averaged over the temperature distributions on the module. This value is quite large, a factor 3 higher than that measured by T. Kondo *et al* . in a thermal study of the "classic r-ϕ module" [6], which indicates that the circulating N_2 gas is much more efficient in convective cooling than stagnant gas. At a power input of 3W through the heater tape, the module picks up 1W from the 0^oC ambient and releases 0.5W into the -10^oC ambient through convection. It should be noted that a power of 1W corresponds to about 2µA/channel at 300V bias, just about the anticipated self heating load after 10 years of operation of ATLAS at the LHC. In the following, we will refer all temperatures to the temperature of the EAR to eliminate the small temperature step between coolant and the EAR.

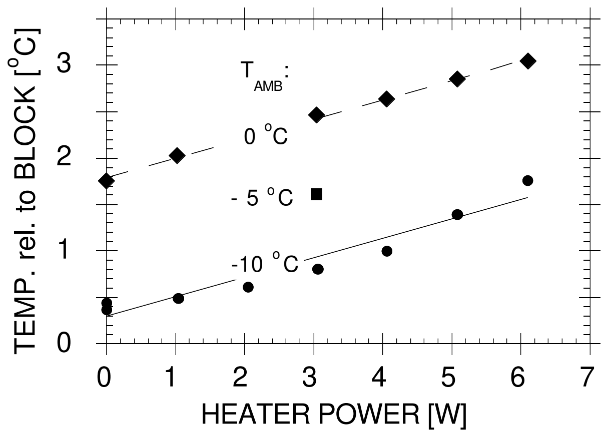

Fig. 6 Temperature of the EAR relative to the cooling block, as a function of the heater tape power, at the three temperatures of the ambient gas, -10, -5 and 0^oC, and coolant at -10^oC.

B. Temperature Profile

We have measured the temperature at several locations on the module as indicated in Fig. 4. Based on tests with the RTD's, we estimate the error to be less than 0.2^oC. In Fig. 7, we show the temperature at RTD #1, which is on the outside of the PG material in between the heater strips on the edge opposite to the EAR.

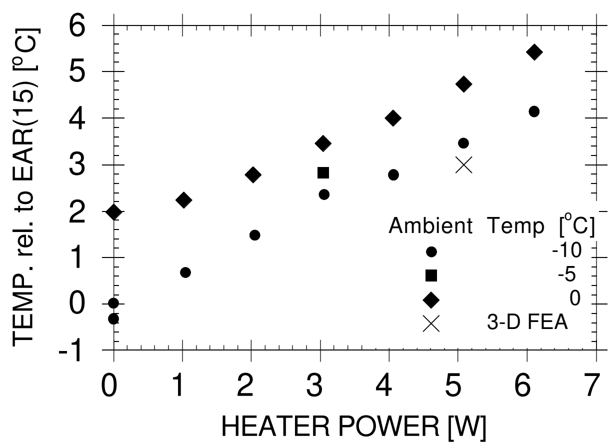

Fig. 7 Temperature of RTD#1 relative to the EAR, as a function of the heater tape power, at three temperatures of the ambient gas: -10, -5 and 0^oC, and coolant at -10^oC.

At an ambient temperature of -10^oC and heater power input of 3W, RTD #1 is 2.4 ^oC above the EAR. At the higher ambient temperature of 0^oC, noticeable convective heating is observed at zero heater power. Thus the temperature increase with increasing ambient at 3W power is not linear. For 5W power input, we have added in Fig. 7 the prediction of a 3-dimensional finite element analysis (FEA) which includes the different materials including the PG heat spreader, the silicon wafers, and glues on the module (but not on the EAR attachment). The simulation was performed assuming the ATLAS chip set mounted on a Kapton hybrid, while we used a heater tape as heat source in our experiment. Thus we would expect differences in the temperature profile in the region of the heater tape. At RTD#1, the data show a temperature of 3.5^{o}C relative to the EAR, while the simulation predicts 3.0^{o}C. Although the agreement is quite good, we will discuss this discrepancy in the following.

In Fig. 8, we compare the measured temperature on several selected RTD location and the prediction of the FEA simulation. The measured data are in the squares on the right, the simulated values on the left. These correspond to a heater power of 3 W and temperatures of -10^{o}C for both the coolant and the ambient gas.

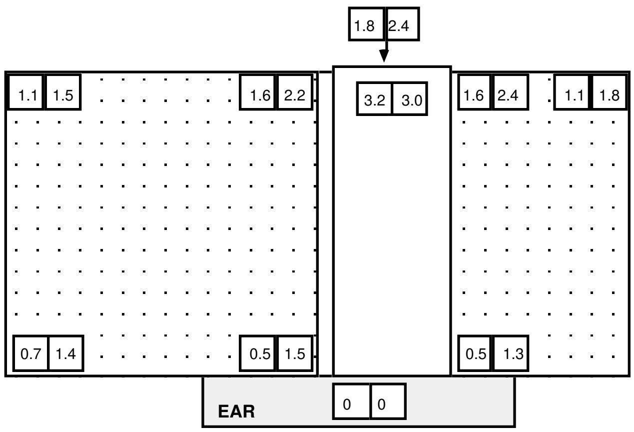

Fig. 8 Temperature profile of the SPGS-module, indicated in the squares. Measured data are on the right, simulated values on the left. Heater tape power=3W, ambient gas and coolant at -10^{o}C.

We notice in Fig. 8 that the temperatures on the module are about 0.6^{o}C higher than predicted. We assume that this is due to our way of constructing the module. One explanation involves the glues which hold the additional pieces of 0.7mm thick carbon fiber material which serve as stiffeners between EAR and cooling block. The epoxy used has a thermal conduction coefficient of about 0.2W/m-^{o}K and thus generates a temperature step, even though the layer is thin and the area of contact is large. We will simply subtract this "temperature step" from the data. The corrected temperature profile is shown in Fig. 9. With the temperature step of 0.6^{o}C removed, the data in Fig. 9 agree very well with the simulation and show about 2^{o}C variation across the module. As mentioned before, the exact temperature of the electronics depends of the exact design of the hybrid.

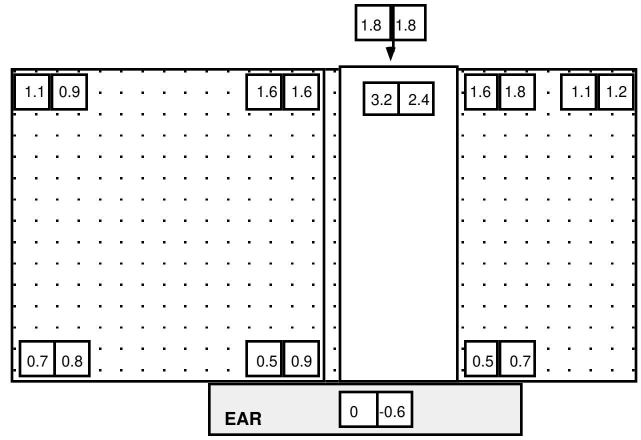

Fig. 9 Temperature profile of the SPGS-module, subtracting the 0.6^{o}C temperature step in the EAR. Measured data are on the right, simulated values on the left. Heater tape power=3W, ambient gas and coolant at -10^{o}C.

IV. CONCLUSIONS

The use of thermally conductive PG material as a heat spreader has been demonstrated experimentally.

The SPGS-module allows safe and predictable removal of heat both from FEE power and from self heating of the detector. The largest temperatures encountered on the thermal prototype are on the Kapton heater and amount to about 3.5^{o}C above the coolant at 3W heater power. The largest temperature difference measured across the silicon module is 1.5^{o}C.

Our results show that the temperature distribution across the module can be simulated reliably with 3-dimensional FEA.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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