Laxmi N. Bhuyan

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Short Biography:

Laxmi Narayan Bhuyan is Professor and Chair of the Computer Science and Engineering Department at the University of California, Riverside. Previously, he was a professor of Computer Science at Texas A&M University (1989-2000) and Program Director of the Computer System Architecture Program at the National Science Foundation (1998-2000). He has also worked as a consultant to Intel and HP Labs.

Dr. Bhuyan received his Ph.D. degree in Computer Engineering from Wayne State University in 1982. His current research interests are in the areas of network computing, multiprocessor architectures, router and web server architectures, parallel and distributed processing, and performance evaluation. He has published more than 150 papers in these areas in IEEE Transactions on Computers (TC), IEEE Transactions on Parallel and Distributed Systems (TPDS), Journal of Parallel and Distributed Computing (JPDC), and many refereed conference proceedings. ***He has made significant contribution to the field of design and analysis of large scale multiprocessors with respect to their interconnections, fault-tolerance, cache coherence protocols, and performance evaluation.***

Dr. Bhuyan currently serves as an Editor-in-Chief of the IEEE Transactions on Parallel and Distributed Systems. In the past, he has served on the Editorial Board of the IEEE TC, JPDC, and Parallel Computing Journal. His professional activities are too numerous to describe. To mention a few, he was the founding Program Committee Chairman of the HPCA in 1995, Program Chair of the IPDPS in 1996, General Chair of ADCOM-2001, General Chair of HPCA-9 (2003), and General Chair of ANCS-2006. He was also elected Chair of the IEEE Computer Society Technical Committee on Computer Architecture (TCCA) from 1995 to 1998.

Dr. Bhuyan is a **Fellow of the IEEE, a Fellow of the ACM, and a Fellow of the AAAS**. He has also been named as an **ISI Highly Cited Researcher** in Computer Science. He has received other awards such as Halliburton Professorship at Texas A&M University, and Senior Fellow of the Texas Engineering Experiment Station. He was also awarded the IEEE CS Outstanding Contribution Award in 1997.

EDUCATION

Ph.D., Computer Engineering, Wayne State University, Detroit, Michigan, 1982.

M.Sc., Engineering (Electrical), Regional Engineering College, Rourkela, Sambalpur University, India, 1979.

B.Sc., Engineering (Hons) (Electrical) - Regional Engineering College, Rourkela, Sambalpur University, India, 1972.

RESEARCH INTERESTS

Computer Architecture, Multiprocessor Cache Memories, Network Processors, Internet Routers, Application Oriented Networking, Parallel and Distributed Computing, Performance Evaluation

PROFESSIONAL EXPERIENCE

July 2007 – Present, Chairman, Department of Computer Science and Engineering, University of California, Riverside.
January 2001- Present, Professor, Computer Science and Engineering, University of California, Riverside.
September 1998-August 2000, Program Director, Computer Systems Architecture, National Science Foundation (NSF).
August 1991-December 2000, Professor, Department of Computer Science, Texas A&M University, College Station, Texas.
August 1998, Consultant, Hewlett-Packard Laboratories, Palo Alto, CA.
Summer 1997, Visiting Professor/Consultant, Intel Corporation, Santa Clara, CA.
Summer 1994, United Nations Development Program (UNDP) Transfer Of Knowledge Through Expatriate Nationals (TOKTEN) Visitor/Consultant to India.
August 1989-August 1991, Associate Professor, Department of Computer Science, Texas A&M University.
August 1985-August 1989, Associate Professor of Computer Engineering, The Center for Advanced Computer Studies, University of Southwestern Louisiana.
August 1983-August 1985, Assistant Professor, Electrical and Computer Engineering, University of Southwestern Louisiana.
September 1982-August 1983, Assistant Professor, Electrical Engineering, University of Manitoba, Canada.

COURSES TAUGHT

Computer Architecture, Advanced Computer Architecture, Performance Evaluation, Computer Design and Implementation, Parallel Computing and Distributed Computer Systems at the graduate level, and Computer Architecture, Operating Systems, Microprocessors, Logic and Switching Circuits at the undergraduate level.

HONORS AND AWARDS

- ***Fellow of the ACM, 2000*** – For significant contributions to the design and analysis of Interconnection Networks and Parallel Processing.
- ***Fellow of the IEEE, 1998*** – For contributions to the design and analysis of interconnection networks and multiprocessor architectures.
- ***Fellow of the AAAS, 2002*** – For contributions to computer architecture and parallel processing.
- ***Fellow of the WIF, 2004 –*** Invited Fellow of the World Innovation Foundation
- ***ISI Highly Cited Researcher, 2002 -*** (among top 250) in Computer Science, 1980-2000.
- **Fulbright Senior Specialist, 2004-2009**
- **Best Paper Award, IFIP Networking 2007**
- *University Partnership Award*, IBM T.J. Watson Research Center, 1998.
- *Golden Core Member*, IEEE Computer Society, 1997.
- *Senior Fellow*, Texas Engineering Experiment Station (TEES), 1996.
- *Outstanding Contribution Award*, IEEE Computer Society, 1996.
- *Fellow*, Texas Engineering Experiment Station (TEES), 1992, 1994.
- *ACM National Lecturer*, 1991-1994.
- *Halliburton Professorship Award*, TAMU College of Engineering, 1991.
- *Distinguished Visitor*, IEEE Computer Society, 1987-90.
- *Best Alumnus Award*, Regional Engineering College, Rourkela, India, 1985.
- *Dean's Honor List*, Wayne State University, Detroit, 1981, 1982.

EDITORIAL ACTIVITIES

- **Editor-in-Chief**, IEEE Transactions on Parallel and Distributed Systems, January 2006 – present
- *Editorial Advisory Board*, International Journal of Parallel, emergent and Distributed Systems, 2006 – present.
- Associate Editor, *IEEE Transactions on Computers*, January 2002 – December 2005
- Editorial Board, *Parallel Computing*, North Holland, 1992 – December 2005
- Area Editor, Performance Evaluation, *Journal of Parallel and Distributed Computing*, 1995 – December 2005.
- Vice Chairman, *IEEE Computer Society Publication Board*, January 2003 - December 2004.
- Member-at-Large, *IEEE Computer Society Publications Board*, 2000 – 2001.
- Associate Editor, *IEEE Transactions on Parallel and Distributed Systems*, 1998 – 1999.
- Area Editor, Systems Architecture, *IEEE Computer*, 1991 - 1997.
- Guest Editor, *Future Generation Computer Systems (FGCS)*, North-Holland, Special Issue on “High-Performance Computer Architecture,” 1995.
- Member, *IEEE CS Publications/Planning Committee*, 1991 - 1992.
- Guest Editor, *IEEE Computer*, Special Issue on ``Interconnection Networks," June 1987.

PROFESSIONAL ACTIVITIES

- *General Chair*, Second IEEE Symposium on Architectures for Networking and Communications Systems (**ANCS**), San Jose, December 2006
- Member, IEEE Fellow Award Committee, 2008
- Steering Committee, ANCS, 2006-present
- *NSF Committee of Visitors (COV),* Computer Networking System (CNS) division, March 2006
- *External Review Panelist*, Computer Science Department, Oklahoma State University, Stillwater, OK, May 2006
- *Vice Chair*, IEEE Computer Society Publications Board, 2003
- *General Co-Chair*, 9th International Symposium on High-Performance Computer Architecture (HPCA), Anaheim, CA, February 2003.
- *General Chair*, IEEE ADCOM, Bhubaneswar, India, December 2001.
- *Advisory Board*, IEEE Technical Committee on Computer Architecture (TCCA), 1995 – present
- *Advisory Committee*, IEEE Technical Committee on Distributed Processing (TCDP), 2001 - present
- *Steering Committee*, International Symposium on High-Performance Computer Architecture, HPCA, 1996 - present.
- *Elected Chair*, IEEE CS Technical Committee on Computer Architecture (TCCA), 1995 - 1998.
- *Member*, ACM/IEEE Eckert-Mauchly Award Subcommittee, 1996 - 1998.
- *Program Co-Chairman*, Eighth IEEE Symposium on Parallel and Distributed Processing (SPDP), 1996.
- *Founding Program Committee Chairman*, International Symposium on High-Performance Computer Architecture (HPCA-1), January 1995.
- *Program Committee*, INFOCOM 2007, Globecom 2006, International Symposium on Computer Architecture (ISCA), 1985,97; International Symposium on High-Performance Computer Architecture (HPCA), 1995,99; International Conference on Parallel Processing (ICPP), 1994,97; Distributed Computing Systems (DCS), 1991,92; IEEE Symposium on Parallel and Distributed Processing (SPDP), 1990,91,93; International Parallel Processing Symposium (IPPS), 1995,98; International Conference on Parallel and Distributed Systems (IPDPS) 2003, Network Computing Applications (NCA) 2001, 2004 and many others.
- *NSF CISE Review Panel*, Computer and Network Systems (CNS) Division, March 2006
- *NSF Site Visitor*, CISE CER Infrastructure Program, Princeton University, 1996
- *International Advisory Panel*, ICAPP-95, Australia; ADCOMP'99, India; CIT'99, India
- *Vice Chairman*, IEEE CS TC on Computer Architecture, 1992 - 1994
- *Panel Moderator*, ISCA International Conf on Parallel & Distributed Systems, 1993
- *Vice Chairman*, International Conference on Distributed Computing Systems, 1992.
- *Tutorial Speaker*, ACM SIGMETRICS Conference, May 1988.
- *Member*, NSF Panel on Research Initiation Awards, 1989, 1992
- *Theme Chair*, ACM Computer Science Conference, 1992
- *Advisor*, USL Chapter of IEEE Computer Society, 1986-1989

RESEARCH ASSOCIATES

- **Dr. R. N. Mahapatra –** Texas A&M University, 1995-2000
- **Dr. Y. Chang –** University of California, Riverside, 2001
- **Dr. Xhiyong Xu** – University of California, Riverside, 2003-2004
- **Dr. In – Bum Jung** – University of California, Riverside, 2004-2005
- **Dr. Bin Liu** – University of California, Riverside, 2006 - 2007

Ph.D. STUDENTS SUPERVISION
(With current appointment)

- **Chita R. Das**, "Dependability Evaluation of Parallel/Distributed Computer Networks," August 1986, (Distinguished Professor at Pennsylvania State University).

- **Qing Yang**, "Analysis of Cache- based Multiple-bus Multiprocessors," August 1988, (Distinguished Professor at University of Rhode Island).

- **Dipak Ghosal**, "A Unified Approach to Performance Evaluation of Dataflow and Multiprocessing Architectures," August 1988, (University of California at Davis).

- **Hong Jiang**, "Performance Evaluation of Shared Memory Multiprocessing Architectures," August 1991, (University of Nebraska-Lincoln).

- **Ashwini K. Nanda,** "Design and Application of Cache Coherent Multiprocessors," May 1993, (IBM TJ Watson Research Center).

- **C.H. Chen**, "Yield and Reliability Aspects of VLSI/WSI Parallel Processing Architectures," May 1993, (University of Tuskegee).

- **Jason Ding**, "Design and Analysis of Buffered Multistage Interconnection Networks," May 1994, (Intel Corporation).

- **Y. Chang**, "Processor Allocation and Fault Tolerance in Multiprocessors," May 1995, (Taiwan).

- **Chao Feng**, "Adaptive Fault-Diagnosis for Multiprocessor Architectures," August 1995, (Motorola Inc.).

- **P.K. Mannava**, "Hypercube Based Shared Memory Multiprocessors," August 1995 (Intel Corporation).

- **Akilesh Kumar**, "Execution Driven Evaluation of Cache Coherent Shared Memory Multiprocessors," May 1996, (Intel Corporation).

- **Ravi Iyer**, "High-Performance Switch Architectures for CC-NUMA Multiprocessors," August 1999, (Intel Corporation).

- **Marius Pirvu,** "Techniques for Reducing Memory Latency in CC-NUMA Multiprocessors," December 2000, (Compaq Corporation).

- **Nan Ni**, "Buffer Management and Fair Scheduling For Input Queued Switches," December 2000, (IBM Corporation).

- **Hu-Jun Wang**, "Efficient Memory Management and Interconnection Schemes for CC-NUMA Multiprocessors", December 2001, (IBM Corporation).

- **Yan Luo,** "Performance Evaluation and Low Power Design of Network Processor", June 2005, (University of Massachusetts at Lowell).

- **Li Zhao**, "Architectural Analysis and Acceleration for Server Network Processing", June 2005, (Intel Corporation).

- **Xiao Zhang**, "Fair Scheduling for Input-Queued Crossbar Switches", August 2005, (Qualcomm).

- **Satya Mohanty, "**Fair Scheduling in Multiple Aggregated Links", April 2007, (Cisco)

- **Jiani Guo**, "Message Scheduling in a Cluster-based Active Router for Multimedia Applications", August 2007, (Cisco)

- **Jia Yu**, "Architectural and Compiler Optimizations for Network Processors", September 2007, (VMWare)

CURRENT Ph.D. STUDENTS

- **Danhua Guo**
- **Yi Hu**
- **Daniel Kuang**
- **Anirban Banerjee** (with Michalis Faloutsos)
- **Guangdeng Liu**

M.S STUDENTS SUPERVISION

Jian Zhou, 2007; S. Mohanty, 2006; C. Baron, 2005; R. Yu, 2000; N. Sudhi, 1999; D. He, 1997; R. Iyer, 1996; K. Shah, 1996; A. Mishra, 1996; M. Holzrichter, 1995; S. Agapito, 1995; M. Kadiyala, 1995; A. Datta, 1994; S. Saheed, 1994; V. Lakamsani, 1993; P. Hangal, 1993; S. Pujari, 1992; T. Askar, 1992; I. Ahmed, 1989; U. Choudhury, 1988; R. Pavaskar, 1988; J. Muppala, 1987; C. Chen, 1987; P. Chuavalee, 1986; S. Berjaouie, 1986; G. Senthilselvan, 1986; P. Pamson, 1985; M. Bharathla, 1985; K. Sureshbabu, 1984; P. Seth, 1984; M. Moghnadam, 1984.

INVITED SEMINARS

- Invited Lecture, Tshinghua University, June 2008
- Invited Lecture, Hong Kong Polytechnic University, June 2008
- **Keynote Speaker**, International Conference on Information Technology (ICIT), India, December 2007
- **Keynote Speaker,** IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS 2007), Boston, Nov 2007
- Invited Lecture, Electrical and Computer Engineering Department, University of Massachusetts, Lowell, November 2007
- **Distinguished Speaker,** Computer Science and Engineering Department, Ohio State University, August 2007
- **Distinguished Speaker**, Electrical Engineering and Computer Science Department, University of California, Irvine, April 2007
- **Bremmer Distinguished Lecturer**, Wayne State University, Detroit, March 2006
- **Keynote Speaker,** First International Conference on Algorithms, Systems, and Applicatiions of Wireless Networks, (WASA'06), Xi'An, China, August 2006
- **Keynote Speaker,** International Workshop on Networks, Architecture and Storage (NAS), Shenyang, China, August 2006.
- Invited Lecture, Tshinghua University, China, August 24, 2006
- Invited Lecture, National Central and Chongking Universities, August 24, 2006
- **Keynote Speaker**, International Conference on Mobile Adhoc and Sensor Networks (MSN), Wuhan, China, December 20, 2005
- **Keynote Speaker**, CIT, Hyderabad, India, December 2004
- Keynote Speaker, International Workshop on Distributed Computing (IWDC), Dec 2003;
- **Distinguished Lecture** at University of Southern California, March 2002;
- Harvey Mudd College, November 2001;
- University of Cincinati, April 2001
- Washington University, October 2000,
- Northeastern University, 2000;
- Southern Methodist University, 1999;
- George Washington University, April 1998;
- HP Laboratories, March 1998;
- **Siemens Distinguished Lecturer**, Florida Atlantic University, 1997;
- IBM T.J. Watson Research Center, October 1997;
- Hewlett Packard Co, Convex Division, Dallas, Spring 1997;
- University of Texas at San Antonio, Spring 1997;
- IBM Corporation, Austin Research Laboratory, Fall 1996;
- Intel Corporation, Santa Clara, Spring 1996;
- Louisiana State University, Dept of Computer Science, Fall 1994;
- Indian Istitute of Technology, Kharagpur, Summer 1994;
- Center for Development of Advanced Computing (CDAC), India, Summer 1994;
- Computer Maintainance Corporation (CMC), India, Summer 1994;
- University of Houston, Dept of Computer Science, Spring 1994;

- Kent State University, Dept of Math and Computer Science, Fall 1993;
- Oklahoma State University, Dept of Computer Science, Spring 1993;
- University of Texas at Arlington, Dept of Comp Sc and Engg, Spring 1993;
- University of Minnesota, Department of Computer Science, Fall 1992;
- University of Nebraska at Lincoln, Department of Computer Science, Fall 1992;
- Indian Institute of Science, Department of Computer Science, Summer 1992;
- University of Texas at Austin, Department of Electrical and Computer Engineering, Spring 1992;
- University of Oklahoma at Norman, Department of Computer Science, Spring 1992;
- University of Houston at Downtown, Mathematics and Computer Science, Spring 1992;
- University of Texas at San Antonio, Mathematics and Computer Science, Spring 1992;
- University of Louisville, Department of Computer Science, Fall 1991;
- North Carolina State University, Electrical and Computer Engineering Department, Spring 1990;
- University of Rhode Island, Department of Electrical Engineering, Fall 1988;
- SUNY at Stony Brook, Department of Electrical Engineering, Spring 1989;
- Rice University, Department of Electrical Engineering, Spring 1989;
- IEEE Computer Society Chapter, Rochester, N.Y. Fall 1988;
- Pennsylvania State University, Department of Electrical Engineering, Fall 1988;
- Wayne State University, Department of Electrical and Computer Engineering, Fall 1988;
- Southern Methodist University, Department of Computer Science, Spring 1988;
- University of Central Florida, Department of Computer Science, Spring 1988.

RESEARCH GRANTS

34. **National Science Foundation**, Principal Investigator, "Virtualization-Aware Architectures to Accelerate Network I/O Processing", $300,000, August 2008 – July 2011.

35. **National Science Foundation**, Principal Investigator, "Application Oriented Edge Router", $410,000, Sept 2008 – August 2011

33. **Intel Corporation,** Principal Investigator, CPU+NIC Architectures to Accelerate I/O Processing, $204,000, July 2007-June 2010.

32. **National Science Foundation**, Principal Investigator, Acquisition of an Ultra Low-Latency Multiprocessor System with On-Board Hardware Accelerators, Equipment Grant, $330,000, August 2006 – July 2009, (with W. Najjar, G. Ciardo, F. Vahid, S. Lonardi and J. Yang).

31. **National Science Foundation**, Principal Investigator, "Collaborative Research: Software Architectures for Distributed Web Services Based on Peer-to-Peer Techniques", Oct 2005 – Sept 2009, $421,586 (UCR portion $275,586), (with Z. Xu, Suffolk University)

30. **National Science Foundation**, Principal Investigator, "Scheduling in High-Performance Internet Routers," $300,000, September 2003 through August 2008.

29. **Cisco**, Principal Investigator "Intelligent Message Scheduling in Application Oriented Networking Systems" $84,000, 2006-07.

28. **UC Micro**, Principal Investigator, Matching for Intel Grant, $38,734, August 2005- December 2006

27. **Intel Corporation**, Principal Investigator, "Advanced Acceleration Solutions for Next Generation Data Center Servers", $64,970, August 2005 -

26. **Intel Corporation**, "Advanced Acceleration Solutions for Next Generation Data Center Servers," $251,617 ($160,000 cash + $91,617 equipment), October 2003, Unrestricted

25. **UC Micro**, "Advanced Acceleration Solutions for Next Generation Data Center Servers," Matching for Intel, $52,536, 2004-2005

24. **Los Alamos National Laboratory, CARE Program**, "Interface Design for High-Performance Networking," $100,000, 2003-2004 (with Mart Molle)

23. **National Science Foundation**, Co-Principal Investigator, "Collaborative Research: Scalable Software System for Large Internet Servers", $441,645 (UCR $186,000 and UC Davis $255,645), March 2003 to February 2007.

22. **Hewlett-Packard Laboratories and UC Micro**, Principal Investigator, "Real-time Scheduling in a Grid Architecture for Interactive and Media Applications", $50,000, January 2003, Unrestricted Gift.

21. **Intel Corporation and UC Micro**, Intel IXA University Program, "Network Processor Laboratory", Principal Investigator, $20,000 Cash + $50,000 Equipment, October 2002, Unrestricted Gift.

20. **National Science Foundation**, Principal Investigator, "ITR: Collaborative Research: Processor Architectures for Web Switches", $486,538 (UCR: $266,538 and UCLA: $220,000), September 2002 through August 2006.

19. **National Science Foundation**, Principal Investigator, "High-Performance Internet Router Architectures", $210,000 + $10,000 (REU), September 2001 through August 2004.

18. **National Science Foundation**, Principal Investigator, "High-Performance Switch Architectures for CC-NUMA Servers," $260,000, January 2001 through August 2004.

17. **Texas Advanced Technology Program**, Principal Investigator, "Architecture Evaluation using Commercial Workloads," $211,750, January 2000 through December 2001.

16. **IBM T.J. Watson Research Center**, University Partnership Award, "Research in Shared Memory Multiprocessor," $29,500 Cash, Unrestricted Gift, 1998.

15. **National Science Foundation**, Principal Investigator, “Cache Coherence in Wormhole Networks,” $258,500, April 1996 to August 2001.

14. **Hewlett-Packard Co**., Principal Investigator, “Research Equipment Grant - 16 Processor V-class Shared Memory Multiprocessor Server,” $1,220,000, January 1998 through December 2000 (with N. Amato and L. Rauchwerger).

13. **Texas Energy Resources Program**, Co-Principal Investigator, “Parallel Processing Algorithms for Rapid Analysis of CT Scan Images,” $25,000, 1998-1999 (with D. Mamora).

12. **Texas A&M System PUF Fund**, Principal Investigator, “Research in Shared Memory Multiprocessors,” $100,000, Equipment Grant, 1997-1998.

11. **National Science Foundation**, Principal Investigator, “Cache Architectures for Large Shared Memory Multiprocessors,” $293,500, July 1993 through June 1996.

10. **Texas Advanced Technology Program**, Principal Investigator, “Fault Tolerance in Multiprocessor Arrays,” $180,000, Jan 1994 through August 1996, (with F. Lombardi).

9. **National Science Foundation**, CISE Small Scale Institutional Infrastructure Program, Co-Principal Investigator, “Research in Parallel and Distributed Computing,” $700,000 NSF + $350,000 TAMU, March 1992 through Feb 1994, (with R. Volz and U. Pooch).

8. **International Business Machines**, Principal Investigator, “Evaluation of Cluster Architectures”, $50,500, Jan 1993 through Dec 1993.

7. **Texas Advanced Technology Program**, Co-Principal Investigator, “An Approach to Solve the Cache Thrashing Problem,” $99,200, Jan 1992 through Dec 1993, (with Mi Lu).

6. **Texas Instruments**, Principal Investigator, “Mapping Algorithms onto Parallel Architectures,” $15,000, 1991, Unrestricted.

5. **National Science Foundation**, Principal Investigator, “Design and Analysis of Cache Coherence Protocols for MIN Based Multiprocessors,” $170,200, Sept. 1990 through August 1993.

4. **National Science Foundation**, Principal Investigator, “Yield and Reliability Considerations of VLSI/WSI based Computing Systems,” $169,200, August 1988 to July 1990, (with T.R.N. Rao and N.F. Tzeng).

3. **LaSER, Board of Regents, Louisiana**, Co-Principal Investigator, “Fault-tolerant Systems and Self Checking Circuits,” $290,000, Jan. 1987 through Dec. 1991, (with T.R.N. Rao).

2. **National Science Foundation**, Co-Principal Investigator, “Fault-tolerance and Reliability of Distributed Computer Systems,” $153,500, March 1986 through August 1988, (with T.R.N. Rao).

1**. NSERC, Canada**, Principal Investigator, “Interconnection Networks for Parallel Computers,” $40,500, April 1983 through March 1986.

PUBLICATIONS

Book Articles

9. Jia Yu, Jun Yang, Shaojie Chen, Yan Luo, and Laxmi Bhuyan, “Enhancing Network Processor Simulation Speed with Statistical Input Sampling”, *Lecture Notes in Computer Science*, Publisher: Springer-Verlag GmbH, ISSN: 0302-9743

8. J. Guo and L. Bhuyan, “Load Balancing in a Transcoding Cluster”, in *Lecture Notes in Computer Science (LCNS), Springer, Vol. LCNS 2918,* 2003, pp. 330-339.

7. Z. Xu, Y. Hu and L. Bhuyan, “HIERAS: A DHT Based Hierarchical P2P Routing Algorithm” *Chapter in High-Performance Computing: Paradigm and Infrastructure*, John Wiley and Sons, 2005, pp. 593-610.

6. L.N. Bhuyan and Y. Chang, “Cache Memory Protocols,” Chapter in *Encyclopedia of Electrical and Electronics Engineering*, Feb. 1999.

5. L.N. Bhuyan and P. Mannava, “High-Performance Computer Architecture,” Chapter in *Encyclopedia in Computer Science and Technology*, Vol. 36, 1997, pp. 173-202.

4. L.N. Bhuyan, Ed., “High-Performance Computer Architecture,” Special Issue in *Future Generation Computer Systems (FGCS)*, North-Holland, Vol. 11, Oct. 1995.

3. L.N. Bhuyan and X. Zhang, Ed., “Multiprocessor Performance Measurement and Evaluation,” *IEEE Computer Society Tutorial*, 1994.

2. D. Ghosal and L.N. Bhuyan, “Performance Evaluation of Dataflow Computers,” Chapter in Dataflow Computing : Theory and Practice, *Ablex Publishing Company,* Ed. by John A. Sharp, 1992.

1. L.N. Bhuyan, Ed., “Special Issue on Interconnection Networks,” *IEEE ComputerMagazine*, Guest Editor, June 1987.

Refereed Journals

57. J. Yao, J. Guo and L. Bhuyan, “Fair Link Striping with FIFO Delivery on Heterogeneous Channels”, *Computer Communications*, Accepted for publication, May 2008

56. J. Yao, J. Guo and L. Bhuyan, “"Ordered Round Robin: An Efficient Sequence Preserving Scheduler for Network Processors" *IEEE Transactions on Computers*, Accepted for publication, April 2008

55. A. Banerjee, M. Faloutsos, and L. Bhuyan, “The P2P War: Someone is Monitoring your Activities” *Computer Networks*, Elsevier Publications, 2008

54. L. Zhao, L. Bhuyan, R. Iyer, S. Makineni, D. Newell, "Hardware support for accelerating data movement in server platform," August, ***IEEE Transactions on Computers***, IEEE, V 56, No. 6, pp. 740-753, June 2007

53. Y. Luo, J. Yu, J. Yang, and L. Bhuyan, "Conserving Network Processor Power Consumption By Exploiting Traffic Variability," ***ACM Transactions on Architecture and Code Optimization (TACO)***, Accepted for publication.

52. J. Guo and L. Bhuyan, “Load Balancing in a Cluster-based Web Server for Multimedia Applications”, ***IEEE Transactions on Parallel and Distributed Systems (TPDS),*** November 2006, pp. 1321-1334.

51. L. Zhao, Y. Luo, L. Bhuyan and R. Iyer, “A Network Processor Based, Content Aware Switch”, ***IEEE Micro,*** Special Issue on High-Performance Interconnects, May/June 2006, pp. 72-84.

50. Z. Xu, L. Bhuyan, and Y. Hu, “Tulip: A New Hash Based Cooperative Web Caching Architecture”, ***The Journal of Supercomputing***, Special Issue on Performance Modelling and Evaluation of Parallel and Distributed Systems, Springer Publication, Volume 35, Number 3, March 2006, pp. 301-320.

49. X. Zhang, L. Bhuyan and W. Feng, “Anatomy of UDP and M-VIA for Cluster Communication” ***Journal of Parallel and Distributed Computing (JPDC),*** Special issue on Design and Performance of Networks for Super-, Cluster-, and Grid-Computing, Vol. 65, Issue 10, October 2005, pp. 1290-1298.

48. R. Iyer, J. Perdue, L. Rauchwerger, N. Amato and L. Bhuyan, “An Experimental Evaluation of the HP V Class and SGI Origin Multiprocessors using Microbenchmarks and Scientific Applications”, ***International Journal of Parallel Programming***, Springer Publications, Vol. 33, No. 4, August 2005, 44 pages.

47. V. C. Ravikumar, R.N. Mahapatra and L.N. Bhuyan, “EaseCAM: An Energy and Storage Efficient TCAM-based Router Architecture for IP Lookup”, ***IEEE Transactions on Computers***, May 2005, pp. 521-533.

46. X. Chen, Y. Luo, H. Hsieh, L. Bhuyan and F. Balarin, "Assertion-Based Verification and Analysis of Network Processor Architectures", ***Design Automation for Embedded Systems,*** Springer Science+Business Publisher, ISSN: 0929-5585, Issue: Volume 9, Number 3, September 2004, Pages: 163 – 176.

45. Y. Luo, J. Yang, L. Bhuyan and L. Zhao, "NePSim: A Network Processor Simulator with Power evaluation Framework" *IEEE Micro, Special Issue on Network Processors*, September/October 2004.

44. Y. Luo, L. Bhuyan and X. Chen, “Shared Memory Multiprocessor Architectures for Software IP Routers”, *IEEE Transactions on Parallel and Distributed Systems (TPDS),* December 2003, pp. 1240-1249.

43. X. Zhang and L.N. Bhuyan, “Deficit Round Robin Scheduling for Input-Queued Switches”, *IEEE Journal on Selected Areas in Communications (JSAC),* Special Issue on "High Performance Optical/Electronic Switches/Routers for High Speed Internet", Vol 21, No. 4, May 2003, pp. 584-594.

42. L. N. Bhuyan and H. Wang, “Switch MSHR: A Technique to Reduce Remote read Memory Latency in CC-NUMA Multiprocessors”, *IEEE Transactions on Computers*, May 2003, Vol. 52, No. 5, pp. 617-632.

41. N. Ni and L.N. Bhuyan, “Fair Scheduling in Input Buffered Switches*” Journal of Cluster Computing, Special Issue on Communication Architectures for Clusters*, April 28, 2003, Vol.6 (2003) No.2, pp. 105-114.

40. R.Iyer, H.Wang, and L. N. Bhuyan, "Design and analysis of Static Memory Management Policies for CC-NUMA Multiprocessors," *Journal of Systems Architecture,* Elsevier Science Publication, 48 (1-3), September 2002, (with R. Iyer and H. Wang).

39. H. Wang, D. Mamora and L.N. Bhuyan, “PPCTSI: A Software Package for Rapid Analysis of CT Scan Images,” *International Journal of Computers and Applications,* Vol. 24, No. 3, 2002.

38. N. Ni and L.N. Bhuyan, “Fair Scheduling in Internet Routers” *IEEE Transactions on Computers, Special issue on on QoS Issues in Internet Web Services*, June 2002, pp. 686-701.

37. R. Iyer and L.N. Bhuyan, “Design and Evaluation of a Switch Cache Architecture for CC-NUMA Multiprocessors,” *IEEE Transactions on Computers,* August 2000, pp. 779-797.

36. L.N. Bhuyan, R. Iyer, H. Wang and A. Kumar, “Impact of CC-NUMA Memory Management Policies on the Performance of Switch Architectures: An Application-Based Study,” *IEEE Transactions on Parallel and Distributed Systems*, March 2000, pp. 230-246.

35. Y. Chang and L.N. Bhuyan, “An Efficient Tree Cache Coherence Protocol for Distributed Shared Memory Multiprocessors,” *IEEE Transactions on Computers*, March 1999, pp. 352-360.

34. L.N. Bhuyan and N. Ni, “Analysis of Interconnection Networks for Cache Coherent Multiprocessors”, Journal of Mathematical Modeling and Scientific Computing, International Association for Mathematical and Computer Modeling (IAMCM), Vol. 8, 1997.

33. J. Ding and L.N. Bhuyan, “Evaluation of Multi-queue Buffered Multistage Interconnection Networks under Uniform and Non-uniform Traffic Patterns,” *International Journal of System Sciences*, Special issue on Distributed Systems, Volume 28, Sept. 1997.

32. L. Bhuyan, R. Iyer, T. Askar, A. Nanda and M. Kumar, “Performance of Multistage Bus Networks for a Distributed Shared Memory Multiprocessor,” *IEEE Transactions on Parallel and Distributed Systems*, January 1997, pp. 82-95.

31. C. Feng, L.N. Bhuyan and F. Lombardi, “Adaptive System-Level Diagnosis for Hypercube Multiprocessors,” *IEEE Transactions on Computers*, V. 45, October 1996, pp. 1157-1170.

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