Long Shaping-time Silicon R&D

ALCPG Tracking Meeting

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Background

Build precise, low-mass silicon central tracker via two developments:

- Stretching signal averages out noise $\Rightarrow$ very long ladders possible; serviced from ends only
- Power-switching to exlpoit $< 1/100$ duty cycle of LC designs

Performance competitive with gaseous tracking over full momentum range

May provide very limited forward material profile

Project Scope

After receiving approval, SCIPP established the following goals for the development of a prototype front-end ASIC

- Characterize semiconductor structures at 0.25 μm.
- Develop pre-amplifier with ability to record min-i particles with 2m, 300 μm-thick, 50 μm-pitch sensors.
- Develop readout (analog, digital?) consistent with goal of finding centroid to 7μm or better.
- Develop power-cycling circuitry to supress IR heating by factor of at least 100.
- Demonstrate noise and power-draw performance with physical 2m-long ladder.

Pukse Development Simulation

Major focus of effort so far (Christian Flacco)

Discovery: much of worry about field modelling, inductive coupling, carrier collection is obviated in long shaping-time limit (whew!).

Want to look at pulse-sharing between strips given a number of variables.

- Magnetic field
- Sensor geometry (pitch, thickness)
- Bias/depletion voltage
- Track incidence (angle, location)

Requires accumulation of understanding of Lorentz angle, mobilities, diffusion (all of which depend on magnetic field).

$\Rightarrow$ Dialog with RD50 to get refined numbers

Looking forward

Hope to have some simulation results by Arlington

Should inform front-end electronic design, esp, decision about analog requirements

Will begin development of 2-m ladders with 'throw-aways' from GLAST

Will possibly begin association with RD50 group to develop large-area sensors via 'Czochralski' process.

Exploring expanded avenues of collaboration with RD50 and through Aurore.

Expecting new post-doc 3/1/03 (Gavin Nesom)