SUPPLEMENTAL ABSTRACT

Long Shaping-Time Silicon Microstrip Readout

Personnel and Institution(s) requesting funding
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There is little question that silicon microstrip tracking will play a central role in any detector that is built for the International Linear Collider. Per radiation length, solid-state tracking provides more precision than gaseous tracking [1], and thus is an integral part of the design of all three detector concepts. One detector design, SiD, plans to make sole use of solid state tracking for its central tracker. The two other designs (GLD, LCD), while nominally employing gaseous central tracking, nonetheless envision silicon microstrip tracking subsystems that approach, and perhaps even exceed, that of the SiD detector in surface area. There is no question that the design of silicon microstrip tracking systems optimized for ILC operating conditions lies directly on the critical path of ILC detector R&D.

The design of such a system will require substantial hardware R&D, including sensitive front-end amplifier/discriminator systems, digital architecture, data transmission, mechanics, and optimized sensor designs. In addition to hardware, though, there is a great need for simulation studies to be carried through, to feed back both into the detailed design of the front-and data-transmission electronics, as well as the geometrical design of the sensors and overall detector. The scope of this proposal is to provide a proof-of-principle of the full electronic readout system (amplifier/comparator, digital architecture, and opto-electronic data transmission), as well as to contribute significantly to the simulation effort, particularly in the arena of understanding pattern recognition issues associated with the use of limited numbers of solid-state tracking layers. This work builds directly on ongoing efforts at the Santa Cruz Institute for Particle Physics (SCIPP), and would extend the reach of ongoing ILC R&D at SCIPP, which can already point to substantial progress in a number of these areas.

At this point, R&D on front-end electronics for ILC detector microstrip readout is underway at three locations: SLAC, LPNHE Paris, and SCIPP. Of these, the SCIPP effort is unique in that it is based on results from a detailed simulation, developed at SCIPP, of the pulse-development, amplification, and readout of microstrip detectors. This has enabled the SCIPP front-end design to focus on the most efficient method of extracting the information associated with locating minimum-ionizing tracks with the greatest possible precision, as well as
providing measurements of ionization energy loss for heavily-ionizing exotic states predicted by a number of plausible extensions of the Standard Model.

This simulation has provided the following guidance:

1) Minimizing readout noise by exploiting slow (long shaping-time) response will allow the use of long sensor ladders (minimizing the amount of material in the active volume) or allow for improved space-point resolution for shorter ladders.

2) Due to the limitations imposed by Landau fluctuations of the deposition in the silicon bulk, it is adequate to obtain analog pulse-height information using a logarithmic time-over-threshold measurement with a minimum time increment of no more than half the shaping time.

3) To adequately suppress detector noise but maintain point-resolution precision when reading out long ladders, it is advantageous to employ two parallel comparator stages for each strip channel: a high threshold comparator to suppress noise, and a lower-threshold comparator to increase the participation of channels neighboring a high-threshold crossing, thus increasing the accuracy of the reconstructed charge-deposition centroid.

The LSTFE-2 chip, now undergoing testing in the SCIPP laboratory, incorporates these features. The shaping-time choice of 3 \( \mu \text{sec} \) represents a compromise between noise performance and the desire to resolve the timing of signal pulses to within several crossing-times of the ILC beam structure. Much of the circuit is functioning at or close to specification, with the preamplifier noise within 20% of design, and the comparator and signal-driving stages functioning as designed. The post-amplification shaping stage is substantially noisier than expectations, and is the focus of our current studies.

To reduce IR heat loss and avoid the need for active cooling of the electronics, the chip is designed so that the power can be switched off in the 200 msec between ILC spills. The LSTFE-2 chip reaches full functionality 20-40 msec after switch-on, resulting in a factor of 5-10 savings in heat production. We are currently exploring ideas that may reduce this by another factor of ten. We expect to submit an upgraded design, incorporating these ideas as well as a solution to the shaper noise problem, by the end of this summer (2006). This re-design will also include a scaling-up from 8 to 128 channels, gearing this next submission towards the development of a prototype tracking system that will be brought to a test beam facility.

In addition to the amplification/comparator development, we have developed a preliminary scheme for processing the digital output of the chip’s comparators. This scheme, to be implemented with an FPGA, will attach time-stamp and channel-number information to each rising and falling transition of the comparator, which will be sampled at the 400 nsec readout clock rate. This information will be stored in a local FIFO that will be read out at the end of each msec ILC beam spill. Transitions of the low-threshold comparator will be read out only if they are nearby in both time and channel number to a rising transition of the high-threshold comparator. Once verified via test beam studies, this digital architecture can be easily translated to the front-end ASIC, eliminating the need for the FPGA (we don’t
consider this pro-forma step to be part of the proof-of-principle though).

The economy provided by strategically limiting the information flow of the system will make the SCIPP scheme simpler and more robust than that of other R&D efforts. In particular, the data rate is modest enough that all the information for a full spill, even for the noisiest inner layer of the detector, can be stored in the local FIFO. Thus, there is no concern about the complication and possible loss of data caused by pipelining – all hits will be recorded for all time slots. Simulation of the SCIPP digital architecture predicts an overall data rate from the tracker of between 0.5 and 5 GHz, depending on the degree of longitudinal segmentation of the tracker. This is well within the capabilities of modern data acquisition systems.

On the simulation front, in addition to the pulse development and digital architecture simulations, the SCIPP group is involved in a number of studies on tracker requirements and performance. The PI of this proposal (Schumm) is the author of LCDTRK [2], a Billior-based track-error calculator that allows for flexible input of detector design parameters. This program has been used extensively by the Linear Collider community in the exploration of detector designs as well as fast Monte Carlo simulations.

A study of selectron production in the SPS1A model [3] (an ILC benchmark process) provided additional motivation for achieving the best possible momentum resolution, and pointed out the particular importance of the forward region in the event that slepton masses are significantly below the ILC beam energy. SCIPP has also been playing an important role in the development and benchmarking of track reconstruction algorithms for the SiD detector concept [4]. Currently, the group is working to combine and optimize complementary tracking algorithms to boost overall SiD tracking performance, and will soon employ this improved algorithm to address basic design issues such as the number and spacing of tracking layers.

While progress on these fronts has been steady, it has been held back by an insufficiency of funds. Currently, the group relies on undergraduate thesis students for a sizeable fraction of the effort. The expertise of senior lab personnel is provided on an as-available basis, and must compete for attention with other, better-funded development projects. One essential issue – that of optical data transmission – has yet to be addressed at all. The availability of supplemental funding would allow us to support these essential lab personnel directly to work on the ILC readout project, as well as to develop the burst-mode optoelectronic system that would be needed to read out the tracker electronics.

In particular, should SCIPP receive sufficient supplemental funding, two new senior members of SCIPP would join the effort. The first of these, Vitaliy Fadeyev, has just joined SCIPP as a Research Physicist, and appears as a co-PI on this abstract. Dr. Fadeyev has extensive experience in the development of front-end electronics and data processing systems for particle physics detector readout. Recently, he has been responsible for LBNL’s development and procurement of the ABCD3T front-end chip for the ATLAS Semiconductor Tracker, as well as refining the data pipelining capabilities of the Hubble Space Telescope’s NICMOS instrument. Dr. Fadeyev’s background is an an excellent match to the work we are proposing in this abstract.

The second senior member of SCIPP that would join the effort if funding were approved is Ken
Pedrotti, who, in addition to his SCIPP affiliation, is an Associate Professor in the UC Santa Cruz Department of Electrical Engineering. Professor Pedrotti, who also appears as a co-PI on this abstract, has extensive background in opto-electronics, at the level of both advanced R&D as well as the more applied level of optoelectronic system design. Professor Pedrotti is interested in the challenges presented by developing a high-bandwidth data transmission system that operates in burst mode to minimize $I^2R$ heat generation. Should we receive money to support an engineering or applied physics graduate student, Professor Pedrotti will supervise this student’s development of a prototype optoelectronic data transmission system that would complete the silicon microstrip readout prototype system we are developing.

**Project Activities and Deliverables**

If solicited to submit a full proposal, we will outline a broad suite of studies that will result in a proof-of-principle for a complete microstrip readout system that would be applicable to any of the ILC detector designs, and would be verified with two test-beam runs in 2008. In addition, we would continue to play a central role in the simulation studies that will refine the SiD detector concept. Assuming that the supplemental funds become available in October 2006, this work will play itself out over the two years from October 2006 through October 2008.

We envision two more submissions of the LSTFE amplifier/comparator chip. The first submission, expected by the end of summer 2006, is expected to resolve the problems with the shaper stage, shorten the time needed to power the chip on, and further improve the signal-to-noise capabilities of the chip. With supplemental funding arriving at SCIPP at roughly the same time as this new (LSTFE-3) version of the amplifier/comparator ASIC, testing could proceed quickly. We would then work towards a second (LSTFE-4) submission by March 2007 that would address any remaining issues with the LSTFE-3 design, as well expand the design to 128 channels in anticipation of use in a test beam. The LSTFE-4 chip would be tested and ready for use in a prototype testbeam system by October 2007, one year into the proposed two-year funding period.

In support of the front-end amplifier/comparator development, we would program the proposed digital scheme onto an FPGA, and test its performance under simulated conditions. This work would also play out over the first year of funding, and should be ready for inclusion in a test-beam prototype system, along with the front-end chip, by October 2007. Once verified in test-beam conditions, we would expect to incorporate this digital scheme onto the front-end ASIC itself, although we don’t consider this final, pro-forma step to be part of the proof-of-principle, and thus are not proposing that this be done on the time scale proposed for the supplemental funding program.

Beginning in Summer 2007, our focus would begin to shift towards the development of a test-beam prototype, to be used in two test-beam runs in early- and mid-2008. The Fermilab Meson Test Beam facility would be a likely host of this run; we have discussed this with Bill Cooper and Marcel Demarteau of FNAL in the past, and they have expressed a willingness to support us in this effort. We are currently exploring the appropriateness of using D0 layer-0
sensors; we have also had some contact with Korean groups doing sensor development geared towards ILC applications. Thus, by the end of the two-year funding cycle (October 2008), we expect to have concrete test-beam results that demonstrate the suitability and advantage of using our readout scheme for ILC microstrip applications.

In parallel with the front-end electronics development, we would begin the program of developing the data-transmission prototype. The elements of this system include parallel-to-serial conversion logic to gather data from multiple amplifier/comparator/FPGA-back-end streams for transmission over a single fiber, opto-electronic circuitry to interface to the output fiber, and handshaking protocols to provide a nearly-instantaneous synchronization with the remote DAQ, to minimize the duty cycle of the data transmission electronics (‘burst-mode operation’). The system must also be engineered with enough redundancy to ensure near-perfect reliability over a 10-year running cycle. It is anticipated that a prototype data transmission system can be designed and assembled by an intermediate-level engineering graduate student, supported by SCIPP staff, and overseen by Professor Pedrotti, an expert in optical communication. A proof-of-principle demonstration of the data transmission system by the end of the funding cycle (October 2008) would be a deliverable of this project.

The SCIPP group has had substantial success in making progress on ILC detector performance simulation with undergraduate and Master’s-level graduate students. Results on detector performance requirements from the SPS1A SUSY benchmark process [3] were performed by UCSC undergraduate students overseen by Schumm. Again overseen by Schumm, important performance benchmarking work on SiD tracking algorithms was done by my Master’s student Michael Young [4], and has been carried on by undergraduate thesis student Eric Wallace, who is also working on further developments of the tracking code itself. Four more students, three of whom expect to be at UCSC for two more years, are now running the ILC simulation framework, and beginning to take on new projects. To date, almost none of this work has been supported by the DOE. (Master’s student Young was supported 1/4-time for one quarter, with the rest of the support coming from the UCSC Physics Department and from SLAC). With relatively minimal additional support, the SCIPP group will contribute to the completion of the refinement of SiD tracking algorithms, and undertake studies to establish the optimal configuration for the SiD tracker.

**Summary**

In all three ILC detector scenarios, silicon microstrip tracking is expected to play a critical role. In this light, SCIPP is proposing a program of R&D on microstrip readout that is unique in breadth. While several institutions are exploring the issue of front-end electronics readout for ILC microstrip detector systems, only the SCIPP program has put forth a picture of the complete readout system, including digital data-handling scheme and optoelectronic data transmission. Furthermore, the intrinsic economy of the SCIPP approach, developed with the aid of a complete simulation of the pulse development and readout scheme, will likely make the SCIPP approach a particularly attractive choice once its capabilities have been demonstrated. Much of the work described in this proposal is underway at some level; even for the least developed part of the system (the optoelectronic readout), several discussions with engineering
faculty have taken place, and while a number of issues remain to be thought through and have their solutions proven, no major roadblocks are seen. To date, the factor providing the greatest impediment to timely progress has been the availability of funds to support dedicated technical staff in this work. The existing funding level (approximately $50,000 per year) has enabled us to submit two preliminary versions of the LSTFE amplifier/comparator chip, but has left little to support these chip’s study and refinement, or to support expansion of the program into other arenas, including the digital architecture, data transmission, and even tracker performance simulation. The availability of supplemental funding provides an opportunity to move forward quickly on these fronts, and to provide a complete proof-of-principle of the SCIPP approach over the two-year time scale of the supplemental funding program.

References
[2] LCDTRK
[3] Troy Lau et al.,
[4] Snowmass tracking simulation paper