Two Solutions to the Miller Effect

Putting a matching resistor on the collector of $Q_1$ would be a big mistake, as it would give no benefit and would produce a severe Miller effect.

For best results, the base of the transistor whose collector has a large voltage swing should be tied to a low impedance source.

Figure 2.74. Two circuit configurations that avoid Miller effect. Circuit B is the cascode.
**Miller Effect**

Base-Collector capacitance together with source impedance forms a low-pass filter, killing the gain at high frequency.

(This voltage divider does nothing but produce heat for the moment.)

**Significant source impedance**

**Exaggerated Base-Source cap**

High gain of ~190 multiplies the 33pF capacitance, making it look like ~6nF!
Response with No Source Impedance
Response with 1kΩ Source Impedance

\[ \frac{1}{2\pi \cdot 1000\Omega \cdot 6\text{nF}} = 26 \text{kHz} \]
Killing the Miller Effect with a Cascode

Within the bandpass, the voltage at this point hardly varies at all, so there is no Miller effect.

Low-impedance (1kΩ) fixed voltage
Cascode Response with 1kΩ Source Impedance
Electronic Noise

- I will skip through this quickly, because most students in Physics 160 are already challenged enough by more basic circuit issues.

- BUT!!

- For a physicist this is often the most critical aspect of circuit behavior that must be well understood and optimized, because
  - amplifiers are likely being used to detect very small signals and
  - noise is unavoidable, tends to be amplified by the amplifier, and can easily obscure the signal.
Thermal Noise

- Thermal noise in a resistance $R$ (Johnson noise):
  - This is the \textbf{minimum} possible noise in any resistance
  - Applies also to dynamic resistances, such as for a diode
  - The power frequency spectrum is flat ("white" noise, up to some limit)

$$\left\langle V_{\text{noise}}^2 \right\rangle = v_n^2 \cdot B \quad \text{with} \quad v_n^2 = 4kTR$$

- $B$ is the \textbf{bandwidth}, which is the frequency range over which you are looking at the noise (e.g. the \textit{maximum} frequency response of your amp or the 60 MHz bandwidth of your lab scope).
  - For example, for an audio amp, $B$ would typically be 20kHz–20Hz, or simply 20kHz.

- \textbf{Low-pass filters are good for reducing white noise, because they reduce $B$.}
  - So don’t make an amp with frequency response that goes way above the signal you are interested in! This is the main reason for the bandwidth-limit button on the lab scope, for example.
Shot Noise

- **Diffusion of electrons across a diode junction is a random process, with each electron acting independently.**
  - This is not the case in a metal wire or a resistor, where the electrons tend to move coherently.

- **If the current is small enough, this stochastic flow can become apparent and appears as random noise called shot noise.**

\[
\langle I_{\text{noise}}^2 \rangle = i_n^2 \cdot B = 2eI \cdot B
\]

- **Note how the power \((I^2R)\) is again proportional to \(B\), indicating that this also is “white” noise.**

- **When the current flows through a resistor, the shot noise naturally gets translated into voltage noise.**

Note that the percentage noise level decreases with increasing current:

\[
\frac{I_{\text{noise}}^{\text{rms}}}{I} = \sqrt{\frac{2e \cdot B}{I}}
\]
Flicker Noise (1/f)

- Excess noise beyond the fundamental thermal and shot noise contributions almost always has a 1/f spectrum (“pink noise”)
  - There is no single physical source of flicker noise, and the amount depends critically on details of the electronic device.
  - It’s not obvious why in general the noise falls like 1/f, but one way or another, the higher frequency noise tends to get suppressed.
  - 1/f means that each decade will have the same noise power.
    - e.g. in an audio amp, the flicker noise power contribution from 20 Hz to 200Hz is the same as from 200 Hz to 2kHz, which is the same as from 2kHz to 20kHz.
  - High pass filters are good for reducing flicker noise.
    - e.g., if we lowered the 3dB point of the audio amp from 20 Hz to 2 Hz, the flicker noise power would go up by 33%.
Transistor (BJT) Noise Model

- **Spice transistor models generally include noise models**
  - But be careful about flicker noise, which often is omitted from the model or set to zero, if you care about low frequencies.
- **Think of the transistor as an ideal noiseless device, but with a voltage noise source in series with the base and a current noise source in parallel with the base-emitter junction.**

Remember, whatever noise is present at the input gets amplified along with the signal!
Transistor Noise

- The source resistance plays two evil roles:
  - It contributes thermal noise, which the amplifier amplifies
  - It converts the shot noise in the base current into voltage, which also gets amplified.
- Thus this transistor model alone contributes an rms noise of

\[ v_{\text{amp (rms)}} = \sqrt{v_n^2 + (R_s \cdot i_n)^2} \]

See the next slide.
Transistor White Noise

Voltage noise:

\[ \nu_n^2 = 4kTr_b + 2eI_C r_e^2 \]

Thermal noise of the intrinsic base resistance (~5 ohms)

Effect of shot noise in the collector current flowing through the intrinsic emitter resistance

\[ \sqrt{4kTr_b} = 0.29 \text{ nV} \quad \text{for } r_b=5 \text{ ohms} \]

\[ \sqrt{2eI_C \cdot r_e} = 0.45 \text{ nV} \quad \text{for } I_C=1 \text{ mA} \]

Current noise:

\[ i_n^2 = 2eI_B \]

Remember:

\[ V_{\text{rms}} = \nu_n \cdot \sqrt{B} \]

\[ I_{\text{rms}} = i_n \cdot \sqrt{B} \]

May 4, 2015  Physics 160
Bias Network Noise

- The bias network contributes noise very differently from the source impedance because it is in parallel with the source, not in series.
  - Therefore, its contribution to $v_n$ will go like $1/\sqrt{R}$, instead of like $\sqrt{R}$.
  - Bootstrapping would essentially eliminate the bias contribution.

The noise current from $R_B$ sees an impedance in this node of $R_S$ in parallel with the amp, so it should be dominated by $R_S$ (i.e. amp $Z_{in} >> R_S$).

The voltage noise of the bias resistor $R_B$ produces a noise current that flows into the amp input node and develops a noise voltage that depends on the impedance of the input node, dominated by $R_S$.

\[
i_n = \frac{\sqrt{4kTR_B}}{R_B}
\]

\[
v_n = \sqrt{\frac{4kT}{R_B}} \times R_S
\]

Note that if there were no source resistance, then this noise source would be insignificant.
Voltage-Amplifier Noise Example

Cascode, to avoid Miller effect and keep gain up to high $f$.  

Scope load

Bypass $R_E$ to get high gain of ~290.

$I_B = 7.7 \mu A$

May 4, 2015 Physics 160
Noise Predictions (referred to the input)

Transistor base: \[ \nu_n = \sqrt{0.29^2 + 0.45^2} \Rightarrow 0.54 \text{nV}/\sqrt{\text{Hz}} \]

Bias network: \[ \sqrt{\frac{4kT}{5.1k}} \times 1k \Rightarrow 1.8 \text{nV}/\sqrt{\text{Hz}} \]

Source resistance: \[ \sqrt{4kT \cdot 1k} \Rightarrow 4.1 \text{nV}/\sqrt{\text{Hz}} \]

Base current: \[ \sqrt{2eI_B} \cdot 1k \Rightarrow 1.6 \text{nV}/\sqrt{\text{Hz}} \]

These 3 contributions go away if the source impedance is zero

Gain \[ \frac{\sqrt{2eI_C \cdot R_C}}{\text{Gain}} = \frac{\sqrt{2e \cdot 1m \cdot 7.5k}}{290} \Rightarrow 0.46 \text{nV}/\sqrt{\text{Hz}} \]

Shot noise of collector current, flowing into the collector load resistor:

Total noise with zero source impedance:
\[ \sqrt{0.54^2 + 0.46^2} = 0.71 \text{nV}/\sqrt{\text{Hz}} \]

Total noise with 1k\(\Omega\) source impedance:
\[ \sqrt{1.8^2 + 4.1^2 + 1.6^2 + 0.71^2} = 4.9 \text{nV}/\sqrt{\text{Hz}} \]
Noise Analysis in PSpice

• Open the simulation settings.
• You can do noise analysis only with the AC Sweep/Noise analysis type.
• Click the box to enable noise analysis.
• Specify the schematic node that represents your output.
• Specify the AC voltage source that is at your input.
• Specify how frequently to print out detailed results (in the ASCII output file). For example, 100 means print details at every 100\textsuperscript{th} frequency.
• Run the analysis.
• Plot $V(\text{ONOISE})$ for the voltage noise spectrum at the output.
• Plot $V(\text{INOISE})$ for the equivalent noise at the input. This is just the output noise divided by the voltage gain.
Spice Analysis with no Source Impedance

Small Signal Gain

Noise at Output

Total noise: \[ \sqrt{(170 \text{nV/Hz})^2 \cdot 10^6 \text{Hz}} = 0.17 \text{mV} \]

Equivalent Noise at Input
Spice Analysis with 1kΩ Source Impedance

**Small-Signal Gain**

Note: the gain is so low in this case because of voltage division between $R_S$ and the bias network.

**Noise at Output**

Total noise: \( \sqrt{\left(\frac{910 \text{nV}}{\sqrt{\text{Hz}}}\right)^2 \cdot 1 \times 10^6 \text{Hz}} = 0.91 \text{mV} \)

**Equivalent Noise at Input**
**Detailed Spice Output at 10kHz**

*High-gain common-emitter amplifier example.*

**FREQUENCY = 1.00E+04 HZ**

**Copied from the PSpice Output File**

**** TRANSISTOR SQUARED NOISE VOLTAGES (SQ V/Hz)

<table>
<thead>
<tr>
<th></th>
<th>Q_Q1</th>
<th>Q_Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>RB</td>
<td>8.595E-15</td>
<td>1.718E-21</td>
</tr>
<tr>
<td>RC</td>
<td>1.748E-22</td>
<td>2.062E-26</td>
</tr>
<tr>
<td>RE</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>IBSN</td>
<td>8.602E-14</td>
<td>1.246E-16</td>
</tr>
<tr>
<td>IC</td>
<td>1.714E-14</td>
<td>7.549E-19</td>
</tr>
<tr>
<td>IBFN</td>
<td>0.000E+00</td>
<td>0.000E+00</td>
</tr>
<tr>
<td>TOTAL</td>
<td>1.118E-13</td>
<td>1.254E-16</td>
</tr>
</tbody>
</table>

*Cascode contributions are negligible*

**These noise voltages all refer to the output, and they are squared per Hz**

**Base current shot noise**

**Collector current shot noise**

**** RESISTOR SQUARED NOISE VOLTAGES (SQ V/Hz)

<table>
<thead>
<tr>
<th></th>
<th>R_RS</th>
<th>R_R2</th>
<th>R_R3</th>
<th>R_RE</th>
<th>R_RLoad</th>
<th>R_R4</th>
<th>R_R5</th>
<th>R_RC</th>
</tr>
</thead>
</table>

*Bootstrapping the bias network would practically eliminate these contributions.*

**Source resistance**

**Bias resistance**

**** TOTAL OUTPUT NOISE VOLTAGE = 8.304E-13 SQ V/Hz

= 9.112E-07 V/RT HZ

= V(ONOISE) in plot

**Transfer Function Value:**  

\[ \frac{V(N00131)}{V_V2} = 1.903E+02 \]

Voltage gain from input to output

**Equivalent Input Noise at V_V2 = 4.788E-09 V/RT HZ = V(INOISE) in plot**

May 4, 2015  
Physics 160  
21
FIELD-EFFECT TRANSISTORS
n-channel MOSFET

- Invented in 1960 at Bell Labs. Infinite DC input impedance!
- All modern computers are based on this device and its p-channel cousin.
- 4-terminal device (gate, drain, source, substrate or body), but often the source is connected internally to the substrate.
- Simplistic explanation: a positive voltage on the gate, relative to the substrate, attracts electrons into the “channel” below the insulator, making it conductive.

![Diagram of an n-channel MOSFET](image)

Both of these diode junctions, source-substrate and drain substrate, must be reverse biased (or zero bias).
CMOS

• Invented in 1963 at Fairchild Semiconductor.
• Manufacture n-channel and p-channel MOSFETs on the same substrate.
• This invention enabled VLSI, with low power consumption.
• In digital switching applications, one transistor is off when the other is on, eliminating essentially all quiescent current.
CMOS ICs

- First CMOS ICs made in 1968 at RCA.
- Modern computer chips have millions of individual transistors.
- To a good approximation, power is only used to charge and discharge capacitance, so the smaller the transistor, the less power it uses and the faster it will switch.
4-Input Multiplexer

Simple example of a logic circuit built up from small gates.
4-input multiplexer VLSI

- 2-input NAND gate
  - poly-silicon gate inputs (blue)
  - layer-2 aluminum metal (2.5 V) (yellow)
  - layer-1 aluminum metal output (cyan)
  - layer-2 aluminum metal (GND) (yellow)
  - NMOS source & drain

- 4-input NOT
  - NMOS source (GND)
  - PMOS source (2.5 V)
  - PMOS drain (output)
  - NMOS drain (output)

- Body contacts
  - GND & 2.5 V

- Layer-3 aluminum metal (green)
  - N-well
Junction FETs (JFET)

- In a JFET the gate is isolated from the channel not by an insulating oxide layer, but instead by a reverse biased PN junction.
- The reverse biased junction will, of course, have a small DC “leakage” current, as is true for any reverse biased PN junction.
- The JFET must always have its gate reverse biased (or zero bias) with respect to the drain and source for it to function!!
- A JFET always works in “depletion mode”. When properly biased, it is normally on, until a voltage is applied to turn it (partially) off.

Note: the source is analogous to the emitter of a BJT, while the drain is analogous to the collector.
MOSFET vs JFET

- Insulated gate can be at any voltage relative to the source, but body must be reverse biased (or zero) w.r.t. the source!
- Both enhancement-mode and depletion-mode are possible, but most often enhancement-mode.
- Zero DC gate current!
- Most widely used as a switch for VLSI digital logic circuits.
- Discrete devices are usually only used for high power transistors and for analog switches.
- Easily destroyed by static electricity!
- 4-terminal device:

- Diode junction gate must be reverse biased (or zero) relative to source!
- Depletion mode only!
- Slight DC gate leakage current.
- Found both as discrete transistors and in ICs (but not VLSI).
  - Current sources or input transistors in op-amps, for example.
- This is the only type used in your FET-1 lab.
- 3-terminal device:

![Diagram of MOSFET and JFET symbols]

May 4, 2015 Physics 160 29